The Invention Claimed Is

1. Apparatus for receiving and processing a CDR signal comprising:

PLD circuitry;

first input circuitry configured to receive the CDR signal;

second input circuitry configured to receive a reference clock signal; and

processing circuitry at least partly controlled by the PLD circuitry and configured to use the reference clock signal to recover data information from the CDR signal.

2. The apparatus defined in claim 1 wherein the PLD circuitry, the first and second input circuitries, and the processing circuitry are all integrated in a single integrated circuit device.

3. The apparatus defined in claim 1 wherein the first input circuitry comprises:

phase locked loop circuitry.

4. The apparatus defined in claim 3 wherein the phase locked loop circuitry is programmable with respect to an operating parameter.

5. The apparatus defined in claim 3 wherein the phase locked loop circuitry is configured to power down in response to a programmable power down signal.

6. The apparatus defined in claim 1 wherein the second input circuitry comprises:

phase locked loop circuitry.

7. The apparatus defined in claim 6 wherein the phase locked loop circuitry is programmable with respect to an operating parameter.

8. The apparatus defined in claim 6 wherein the phase locked loop circuitry is configured to power down in response to a programmable power down signal.

9. The apparatus defined in claim 6 wherein the first input circuitry comprises:

further phase locked loop circuitry configured to receive an output signal of the phase locked loop circuitry and to produce a recovered clock signal that is synchronized with the CDR signal.

10. The apparatus defined in claim 9 wherein the further phase locked loop circuitry is further configured to adjust the phase of the output signal of the phase locked loop circuitry to produce the recovered clock signal.

11. The apparatus defined in claim 1 wherein the processing circuitry comprises:

deserializer circuitry configured to convert the data information from serial to parallel form.

12. The apparatus defined in claim 11 wherein the deserializer circuitry is programmable with respect to an operating parameter.

13. The apparatus defined in claim 11 wherein the deserializer circuitry is further

configured to reset in response to a reset signal selectively produced by the PLD circuitry.

14. The apparatus defined in claim 1 wherein the processing circuitry comprises:

buffer circuitry configured to buffer the data information between a clock regime associated with reference clock signal and a different clock regime.

15. The apparatus defined in claim 14 wherein the buffer circuitry is further configured to reset in response to a reset signal selectively produced by the PLD circuitry.

16. The apparatus defined in claim 1 wherein at least one of the first input, second input and processing circuitries is configured to apply to the PLD circuitry a condition-monitoring signal indicative of an operating condition of that at least one circuitry.

17. The apparatus defined in claim 1 wherein at least one of the first input, second input, and processing circuitries includes a component that is reset by a reset signal selectively produced by the PLD circuitry.

18. The apparatus defined in claim 1 wherein the first input circuitry is further configured for alternate use to receive a non-CDR data signal; the second input circuitry is further configured for alternate use to receive a non-CDR clock signal that is synchronized with the non-CDR data signal; and the

processing circuitry is further configured for alternate use to derive the data information from the non-CDR data signal using the non-CDR clock signal.

19. The apparatus defined in claim 18 wherein the non-CDR data signal is an LVDS signal.

20. The apparatus defined in claim 1 further comprising:

output circuitry configured to receive further data information from the PLD circuitry and to use the reference clock signal to encode the further data information as a further CDR signal for output by the apparatus.

21. The apparatus defined in claim 20 further comprising:

loopback circuitry configured to selectively use the further CDR signal as the CDR signal.

22. The apparatus defined in claim 21 wherein the loopback circuitry is configured so that it can be controlled by a signal from the PLD circuitry.

23. The apparatus defined in claim 20 further comprising:

loopback circuitry configured to selectively route the CDR signal for output by the apparatus in lieu of the further CDR signal.

24. The apparatus defined in claim 23 wherein the loopback circuitry is configured so that it can be controlled by a signal from the PLD circuitry.

25. The circuitry defined in claim 21 wherein the loopback circuitry is further configured for selective control by the PLD circuitry.

26. Apparatus for producing and transmitting a CDR signal comprising:

PLD circuitry configured to produce data information;

input circuitry configured to receive a reference clock signal; and

output circuitry configured to use the reference clock signal to produce the CDR signal including the data information.

27. The apparatus defined in claim 26 wherein the PLD circuitry, the input circuitry, and the output circuitry are all integrated in a single integrated circuit device.

28. The apparatus defined in claim 26 wherein the input circuitry comprises:

phase locked loop circuitry.

29. The apparatus defined in claim 28 wherein the phase locked loop circuitry is programmable with respect to an operating parameter.

30. The apparatus defined in claim 28 wherein the phase locked loop circuitry is configured to power down in response to a programmable power down signal.

31. The apparatus defined in claim 26 wherein the output circuitry comprises:

buffer circuitry configured to buffer the data information between a clock regime associated with the PLD circuitry and a different clock regime associated with the reference clock signal.

32. The apparatus defined in claim 26 wherein the output circuitry comprises:

serializer circuitry configured to convert the data information from parallel to serial form.

33. The apparatus defined in claim 32 wherein the serializer circuitry is programmable with respect to an operating parameter.

34. The apparatus defined in claim 26 wherein at least one of the input and output circuitries is configured to apply to the PLD circuitry a condition-monitoring signal indicative of an operating condition of that at least one circuitry.

35. The apparatus defined in claim 26 wherein at least one of the input and output circuitries includes a component that is reset by a reset signal selectively produced by the PLD circuitry.

36. The apparatus defined in claim 26 wherein the PLD circuitry is further configured to produce a non-CDR clock signal synchronized with the data information, and wherein the output circuitry is further configured for alternative use in outputting the data information in non-CDR form in parallel with the non-CDR clock signal.

37. The apparatus defined in claim 36 wherein the output circuitry is further configured to selectively frequency-scale the non-CDR clock signal by a predetermined scale factor prior to outputting the non-CDR clock signal in frequency-scaled form.

38. The apparatus defined in claim 37 wherein the output circuitry is programmable with respect to the scale factor.

39. The apparatus defined in claim 36 wherein the non-CDR form of the data information is an LVDS signal.

40. Apparatus for receiving an information signal which includes data information having clock information for the data information embedded in the data information comprising:

first input circuitry configured to receive the information signal;

second input circuitry configured to receive a reference clock signal having a reference frequency which is related to a frequency of the clock information by a predetermined scale factor;

reference clock signal processing circuitry configured to use the information signal and the reference clock signal to produce a recovered clock signal having phase and frequency which respectively correspond to a phase and a frequency of the clock information; and

data recovery circuitry configured to use the recovered clock signal and the information signal to produce a data output signal indicative of the data information in the information signal.

41. The apparatus defined in claim 40 further configured to be programmable with respect to the scale factor.

42. The apparatus defined in claim 40 further comprising:

deserializer circuitry configured to convert the data output signal to a plurality of parallel data subsignals, each of which represents a respective portion of the data information indicated by the data output signal.

43. The apparatus defined in claim 42 wherein the deserializer circuitry is programmable with respect to how many parallel data subsignals are produced.

44. The apparatus defined in claim 40 further comprising:

synchronizer circuitry configured to convert the data output signal to a further data output signal synchronized with a read control signal which can have phase and frequency substantially unrelated to the phase and frequency of the reference clock signal and the recovered clock signal.

45. The apparatus defined in claim 44 further comprising:

selection circuitry configured to select as a final data output signal either the data output signal or the further data output signal.

46. The apparatus defined in claim 40 wherein the reference clock signal processing circuitry

is further configured to use the scale factor in producing the recovered clock signal.

47. The apparatus defined in claim 46 wherein the reference clock signal processing circuitry is programmable with respect to the scale factor.

48. The apparatus defined in claim 40 wherein the information signal is applied to the first input circuitry as a pair of differential signals, and wherein the first input circuitry comprises differential driver circuitry configured to use the differential signals to produce a single output signal for further processing by the apparatus.

49. The apparatus defined in claim 40 wherein the reference clock signal is applied to the second input circuitry as a pair of differential signals, and wherein the second input circuitry comprises differential driver circuitry configured to use the differential signals to produce a single output signal for further processing by the apparatus.

50. The apparatus defined in claim 40 wherein the reference clock signal processing circuitry comprises:

phase locked loop circuitry configured to use the reference clock signal and the scale factor to produce a plurality of candidate further reference clock signals, each having the frequency of the clock information and having a phase which is different from the phases of all the other candidate further reference clock signals.

51. The apparatus defined in claim 50 wherein the reference clock signal processing circuitry further comprises:

further phase locked loop circuitry configured to use the information signal and the candidate further reference clock signals to produce the recovered clock signal.

52. The apparatus defined in claim 51 wherein the further phase locked loop circuitry comprises:

selection circuitry configured to select as the recovered clock signal the one of the candidate reference clock signals having the phase that works best with the phase of the clock information.

53. The apparatus defined in claim 40 wherein the data recovery circuitry comprises:

register circuitry having a data input terminal to which the information signal is applied and a clock input terminal to which the recovered clock signal is applied, the register circuitry being configured to store and output samples of the signal applied to the data input terminal in synchronism with the signal applied to the clock input terminal.

54. The apparatus defined in claim 53 wherein the data recovery circuitry further comprises:

buffer memory circuitry configured to store multiple successive signal samples output by the register in synchronism with the recovered clock signal and to output those samples in the same order in response to another separate read clock signal.

55. The apparatus defined in claim 40 wherein the information signal represents successive words of J serial bits of data, and wherein the data recovery circuitry comprises:

shift register circuitry having a plurality of serially connected stages and configured to shift in successive samples of the information signal in synchronism with the recovered clock signal;

frequency divider circuitry configured to divide the recovered clock signal by J to produce a further reference clock signal; and

unload circuitry configured to unload all stages of the shift register circuitry in parallel word form in synchronism with the further reference clock signal.

56. The apparatus defined in claim 55 wherein the frequency divider circuitry is programmable with respect to J.

57. The apparatus defined in claim 55 wherein the data recovery circuitry further comprises:

buffer memory circuitry configured to store multiple successive parallel words from the unload circuitry in synchronism with the still further reference clock signal and to output those parallel words in a same order in response to another separate read clock signal.

58. The apparatus defined in claim 40 further comprising:

PLD circuitry configured to use the data output signal.

59. The apparatus defined in claim 58 wherein all of the circuitries are disposed on a single integrated circuit.

60. The apparatus defined in claim 58 further comprising:

routing circuitry configured to selectively apply a signal indicative of the recovered clock signal to the PLD circuitry.

61. The apparatus defined in claim 44 further comprising:

PLD circuitry configured to produce the read control signal.

62. The apparatus defined in claim 61 wherein the PLD circuitry is further configured to use the data output signal.

63. A signaling system comprising:

the apparatus defined in claim 40;

a first source of the information signal;

a second source of the reference clock signal;

a first connection between the first source and the first input circuitry; and

a second connection between the second source and the second input circuitry.

64. The system defined in claim 63 wherein the first and second input circuitries are disposed on a common integrated circuit which does not also include the first and second sources.

65. The apparatus defined in claim 40 wherein the information signal is a clock data recovery signal.

66. The apparatus defined in claim 40 further comprising:

alternative reference clock signal processing circuitry configured to selectively alternatively produce a further reference clock signal based on the reference clock signal and without regard for the information signal.

67. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

apparatus as defined in claim 40 coupled to the processing circuitry and the memory.

68. A printed circuit board on which is mounted apparatus as defined in claim 40.

69. The printed circuit board defined in claim 68 further comprising:

a memory mounted on the printed circuit board and coupled to the apparatus.

70. The printed circuit board defined in claim 68 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the apparatus.

71. Apparatus for transmitting an information signal which includes data information

having clock information for the data information embedded in the data information comprising:

input circuitry configured to receive a reference clock signal having a reference frequency which is related to a frequency of the clock information by a predetermined scale factor;

reference clock signal processing circuitry configured to use the reference clock signal to produce a further reference clock signal having the frequency of the clock information;

data source circuitry configured to produce a data signal indicative of the data information; and

data signal processing circuitry configured to process the data signal in accordance with the further reference clock signal to produce the information signal.

72. The apparatus defined in claim 71 further configured to be programmable with respect to the scale factor.

73. The apparatus defined in claim 71 wherein the data source circuitry is configured to produce the data signal as a plurality of parallel data subsignals, each of which represents a respective portion of the data information, and wherein the data signal processing circuitry comprises:

serializer circuitry configured to convert the plurality of parallel data subsignals to a single serial data signal.

74. The apparatus defined in claim 73 wherein the serializer circuitry is programmable with

respect to how many parallel data subsignals are converted.

75. The apparatus defined in claim 71 wherein the data signal processing circuitry comprises:

synchronizer circuitry configured to receive the data signal in synchronism with a write control signal and to subsequently output the data signal in synchronism with the further reference clock signal, wherein the write control signal can have phase and frequency which are substantially unrelated to the phase and frequency of the reference clock signal and the further reference clock signal.

76. The apparatus defined in claim 75 wherein the data signal processing circuitry further comprises:

selection circuitry configured to allow the data signal to selectively bypass the synchronizer circuitry.

77. The apparatus defined in claim 71 wherein the reference clock signal processing circuitry is further configured to use the scale factor in producing the further reference clock signal.

78. The apparatus defined in claim 77 wherein the reference clock signal processing circuitry is programmable with respect to the scale factor.

79. The apparatus defined in claim 71 wherein the reference clock signal is applied to the input circuitry as a pair of differential signals, and wherein the input circuitry comprises differential

driver circuitry configured to use the differential signals to produce a single output signal for further processing by the apparatus.

80. The apparatus defined in claim 71 wherein the data signal processing circuitry comprises differential driver circuitry configured to transmit the information signal as a pair of differential signals.

81. The apparatus defined in claim 71 wherein the reference clock signal processing circuitry comprises:

phase locked loop circuitry configured to use the reference clock signal and the scale factor to produce the further reference clock signal.

82. The apparatus defined in claim 71 wherein the data signal processing circuitry comprises:

register circuitry having a data input terminal to which the data signal is applied and a clock input terminal to which the further reference clock signal is applied, the register circuitry being configured to store samples of the signal applied to the data input terminal and to output those samples in synchronism with the signal applied to the clock input terminal.

83. The apparatus defined in claim 71 wherein the data signal comprises a plurality of parallel data subsignals, each of which is indicative of a portion of the data information, and wherein the data signal processing circuitry comprises:

register circuitry having a plurality of data input terminals to which the data subsignals are respectively applied and a clock input terminal to which the further reference clock signal is applied, the register circuitry being configured to store samples of the signals applied to the data input terminals and to output those samples in series in synchronism with the signal applied to the clock input terminal.

84. The apparatus defined in claim 83 wherein the data signal processing circuitry further comprises:

buffer memory circuitry configured to store multiple successive samples of each of the data subsignals in response to another separate write clock signal and to output those samples in the same order in synchronism with the further reference clock signal.

85. The apparatus defined in claim 83 wherein the plurality of parallel data subsignals comprises J parallel data subsignals, and wherein the register circuitry comprises:

shift register circuitry having a plurality of serially connected stages and configured to shift out contents of those stages in series in synchronism with the further reference clock signal;

frequency divider circuitry configured to divide the further reference clock signal by J to produce a still further reference clock signal; and

load circuitry configured to load, in parallel, all stages of the shift register circuitry with samples of the data subsignals in synchronism with the still further reference clock signal.

86. The apparatus defined in claim 85 wherein the frequency divider circuitry is programmable with respect to J.

87. The apparatus defined in claim 85 wherein the register circuitry further comprises:

buffer memory circuitry configured to store multiple successive parallel words of samples of the data subsignals in response to another separate write clock signal and to output those parallel words in a same order in response to the still further reference clock signal.

88. The apparatus defined in claim 71 wherein the data source circuitry comprises PLD circuitry.

89. The apparatus defined in claim 88 wherein all of the circuitries are disposed on a single integrated circuit.

90. The apparatus defined in claim 88 further comprising:

routing circuitry configured to selectively apply a signal indicative of the further reference clock signal to the PLD circuitry.

91. The apparatus defined in claim 75 further comprising:

PLD circuitry configured to produce the write control signal.

92. The apparatus defined in claim 91 wherein the PLD circuitry is further configured to include the data source circuitry.

93. A signaling system comprising:

the apparatus defined in claim 71;

a first source of the reference clock signal;

a second receiver of the information signal;

a first connection between the first source and the input circuitry; and

a second connection between the data signal processing circuitry and the second receiver.

94. The system defined in claim 93 wherein the input circuitry and the data signal processing circuitry are disposed on a common integrated circuit which does not also include the first source and the second receiver.

95. The apparatus defined in claim 71 wherein the information signal is a clock data recovery signal.

96. The apparatus defined in claim 71 further comprising:

alternative reference clock signal source circuitry configured to produce an alternative clock signal;

signal selection circuitry configured to allow the alternative clock signal to be alternatively selectively used by the data processing circuitry as the further reference clock signal; and

output circuitry configured to output the alternative clock signal in parallel with the information signal.

97. The apparatus defined in claim 96 wherein the data signal processing circuitry comprises first differential driver circuitry configured to transmit the information signal as a first pair of differential signals, and wherein the output circuitry comprises second differential driver circuitry configured to transmit the alternative clock signal as a second pair of differential signals.

98. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

apparatus as defined in claim 71 coupled to the processing circuitry and the memory.

99. A printed circuit board on which is mounted apparatus as defined in claim 71.

100. The printed circuit board defined in claim 99 further comprising:

a memory mounted on the printed circuit board and coupled to the apparatus.

101. The printed circuit board defined in claim 99 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the apparatus.

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